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Title of the Invention

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

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SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

Field of the Invention

The present invention relates to an oscillation circuit, and a semiconductor integrated circuit device which includes a clock distribution system of low jitter and low skew employing the oscillation circuit.

Background of the Invention

A clock generation method which uses a conventional PLL (Phase-locked loop) is disclosed in, for example, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL 27, NO 11, November 1992 (hereinbelow, referred to as the "prior art example A").

Fig. 2 illustrates the construction of a clock generation unit which employs the conventional PLL. A reference clock signal fext input to the PLL from outside the circuit. The PLL includes the following: "PFD", a phase/frequency comparator; "CP", a charge pump; "LPF", a low-pass filter; "VOC0", a voltage-controlled oscillator; "DIVN", a 1/N frequency divider; "DIV2", a 1/2 frequency divider; and "N0", a clock distribution network. The details of each of these circuit elements is omitted.

The difference between the phases or frequencies of the reference clock signal fext and an internal clock signal fint is compared by the phase/frequency comparator PFD, from which an error signal UP or DN is output. The error signal is converted into an analog signal by the charge pump CP, and the high frequency components of the signal are removed by the low-pass filter LPF. The resulting signal is input to the voltage-controlled oscillator VCO0 as an oscillation-frequency control signal VC. The oscillation output of the voltage-controlled oscillator VCO0 is divided by the frequency divider DIV2 into an oscillation output fint0 whose frequency is half the frequency of the former oscillation output and whose duty

ratio is 50%, and which is input to the clock distribution
network N0.

The return signal fint from the clock distribution system
has its frequency divided by the 1/N frequency divider DIVN.
The resulting signal is input to the phase/frequency
comparator PFD. The phases of the reference clock fext and
internal clock fint are locked by such a phase-locked loop
PLL0, and the frequency of the signal fint becomes N times
that of the signal fext.

Summary of the Invention

The frequency of the internal clock fint has increased
year by year, and the area of the clock distribution network
N0 has been enlarged in accordance with increases in chip
area. Problems occur in a clock distribution system when the
clock is to be stably fed at high speed over a wide area.
Such problems, as mentioned below, occur with the prior art
Example A.

(1) The delay time of the clock distribution network,
that is, the delays in the signals fint0 and fint, become(s)
relatively long in comparison with 1/fint. Thus, the skew of
the clock distribution network influences the performance of
the whole clock distribution system into which the clock
distribution network and the phase-locked loop PLL0 are
combined. Also, there is a method wherein a clock feed range
within a chip is split in a large number, and wherein
independent PLLs are provided for the respective clock feed
subranges. In the case of this method, however, problems as
mentioned below are involved.

(2) In general, a PLL is less immune to noise such as
power source noise and substrate noise, and such noise
increases the "jitter" of the oscillation frequency and phase
of the signal fint0. The provision of the large number of

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PLLs within the chip leads to the necessity of considering noise reduction for each of the PLLs.

(3) The total area of the large number of PLLs affects the area of the entire chip. In consideration of the problem (2), the area of each of the PLLs increases even more.

(4) The clock skew between the independent clock feed subranges becomes as very large as $TskewG + 2*TskewL + 2*Tjitter$, where TskewL denotes a skew within the respective clock feed subranges, Tjitter denotes the jitter of the PLLs, and TskewG denotes the skew of the reference clock having occurred up to each PLL.

(5) Since the PLLs are provided in such a large number, dissipation power increases.

The objects of the invention are to solve the aforementioned problems by providing an oscillation circuit and a semiconductor integrated circuit device which includes a clock distribution system using the oscillation circuit.

In particular, it is an object of the invention to provide a semiconductor integrated circuit device having a plurality of oscillators each having an oscillation node, wherein the oscillation nodes of each of the oscillators are connected together. Preferably, the oscillators are connected together by conductive wiring line that may be a closed loop.

It is a further object of the invention that the oscillators are synchronized to oscillate at substantially the same frequency and further to oscillate at substantially the same phase.

It is another object of the invention that the oscillators are connected to a wiring at connecting points having substantially the same interval of wiring lengths between the connection points, which leads to synchronizing the oscillators to oscillate at a substantially identical frequency and phase.

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In a preferred embodiment of the invention, the semiconductor integrated circuit device has a plurality of oscillators that are connected to a conductive wiring line that is formed in the shape of a mesh, at the intersection points of the mesh, wherein the interval of length of the conductive wiring line between the connection points is substantially the same among all of the connection points. Preferably, the interval length is at least 50 μm.

In a further object of the present invention, the oscillators are ring oscillation circuits having inverters connected in a ring shape wherein an output of at least one inverter of each ring oscillation circuit is connected to the conductive wiring. Alternatively, the oscillators may be delay lines having multistage connected inverters with at least one inverter connected to the conductive wiring line.

According to another object of the invention, a semiconductor integrated circuit device is provided with a plurality of circuit blocks having a clock distribution circuit and a plurality of oscillators that output a clock signal to the clock distribution circuit in which a conductive wiring is provided for connecting oscillation nodes of each of the oscillators together. In such an arrangement, the circuit blocks may comprise a logic circuit or a memory circuit and the plurality of oscillators may be provided in one-to-one correspondence with the plurality of circuit blocks.

In still another object of the invention, a semiconductor integrated circuit device has a plurality of oscillation circuits with a wiring connecting the output of oscillation circuits together, a plurality of clock distribution circuits that are connected to the oscillation circuits and a phase frequency converter that compares the clock signal of the clock distribution circuits with a reference clock signal wherein the oscillation circuits change in oscillation

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frequency in response to a signal output from a phase frequency comparator.

According to the present invention, a semiconductor integrated circuit device is provided having a plurality of oscillators having substantially the same natural oscillation frequency and a conductive wiring that connects the outputs of each of the oscillators together. As a result, the oscillators oscillate at substantially the same frequency independently of fluctuations in the supply of voltage to each of the oscillators. Further, since the oscillators are synchronized to provide substantially the same output frequency which is independent of fluctuations in the supply voltages, the oscillators are suitable for providing a clock signal to a plurality of clock distribution circuits that distribute clock signals to circuit blocks on the semiconductor integrated circuit device. As a result, a clock signal is provided that is distributed according to the preferred embodiments of the invention that is not subject to variations due to noise and therefore has low jitter and skew.

Brief Description of the Drawings

Fig. 1 is a diagram showing the basic embodiment of the present invention.

Fig. 2 is a diagram showing a clock generation unit which employs a conventional PLL.

Fig. 3 shows graphs illustrating the circuit simulation waveforms of the oscillation circuits according to the present invention.

Fig. 4 is a diagram of an embodiment in which ring oscillators are connected to separate power sources in an oscillation circuit of the present invention.

Fig. 5 is a diagram of an embodiment pf an oscillation circuit according to the invention in which differential inverters are employed in the ring oscillators.

Fig. 6 is a diagram of an embodiment of the invention showing a different connection than that shown for the embodiment of Fig. 1.

Fig. 7 is a diagram of an embodiment of the invention showing a different connection than that shown for the embodiment of Fig. 1.

Fig. 8 is a diagram of an oscillation circuit embodiment of the invention in which ring oscillators are connected to a mesh in the shape of an array.

Fig. 9 is a diagram of an embodiment in which clocks are fed to a plurality of logic circuits by the use of the oscillator of the present invention.

Fig. 10 is a diagram of an embodiment according to which, in the invention of Fig. 9, the phases of the clocks for the respective logic circuits are made to be adjustable.

Fig. 11 is a diagram of an embodiment in which the oscillator of the present invention are used as voltage-controlled oscillators (variable-frequency oscillators) in a phase locked loop PLL circuit.

Fig. 12A is a diagram showing a basic embodiment of a voltage-controlled oscillator.

Fig. 12B is a diagram showing another basic embodiment of a voltage-controlled oscillator.

Fig. 13 is a diagram of a basic embodiment of a clock distribution network according to the present invention.

Fig. 14 is a diagram of a microprocessor according to the present invention.

Fig. 15 is a diagram of an embodiment in which the present invention is applied to delay lines.

Fig. 16 is a diagram of an embodiment in which a delayed lock loop (DLL) is constructed using voltage-controlled delay lines (variable delay lines) as the delay lines in Fig. 15.

Fig. 17A is diagram of the embodiment of the invention shown in Fig. 8 with switches interposed between the connection points of the mesh.

Fig. 17B is a diagram of a switch used in the embodiment of Fig. 17B.

Fig. 18 is a diagram of an embodiment similar to that of Fig. 8 with PLLs used in place of the ring oscillator shown in Fig. 8.

Fig. 19 is a diagram of an embodiment of the PLLs used in Fig. 18.

Detailed Description of the Preferred Embodiments

Fig. 1 is a diagram showing a basic embodiment of the oscillation circuit of the present invention, which includes ring oscillators OSC1 - OSCn, which are respectively configured of inverters 110 - 11m, 120 - 12m, and 1n0 - 1nm. One of the oscillation nodes of each of the ring oscillators is connected to the corresponding one of nodes 101 - 10n, and the adjacent nodes 101 - 10n are connected together by the wiring, which is preferably in a closed loop shape. Also, preferably, the interval of wiring length or distance between the adjacent nodes (for example, the distance between the nodes 101 and 102) are equal distances 1. The inverters 110 - 11m, 120 - 12m, and 1n0 - 1nm may be CMOS inverters, although not limited thereof. For the sake of brevity, inverters of the CMOS type are described as employed in the description of Fig. 1 below.

Since the oscillation nodes of the respective ring oscillators OSC1 - OSCn are connected with one another, these ring oscillators OSC1 thru OSCn oscillate at a substantially identical phase/frequency.

Fig. 3(A) illustrates circuit simulation waveforms in the
case where the number of ring oscillators is four. The axis
of abscissa represents the time, while the axis of ordinate
represents the voltages of the respective nodes. In the
figure, V(x), i.e. V(101), V(102), etc. denotes the potential
of the node x. Transistors used in the simulation were CMOS
transistors each of which had a gate length Lg of 0.25 μm.
The inverters 110 - 11m, 120 - 12m, and 1n0 - 1nm were all the
same type of inverters (in which the gate width Wp of each
PMOS transistor was 10 μm, and the gate width Wn of each NMOS
transistor was 5 μm). A supply voltage was 1.8 V, and the
distance l between the nodes was 3 mm. It was assumed that in
an initial state, the respective nodes 101 - 104 had different
potentials as their initial values (at the point of time of 0
ns). It is seen that, although there were in different phases
at the time point 0 ns, the ring oscillators OSC1 thru OSC4
oscillated in and at an identical phase/frequency in a steady
state established after a while subsequent to time point 0 ns.

In this manner, as a result of the configuration of the
present invention, the ring oscillators, the adjacent ones of
which are spaced apart from one another by the distance l, can
be caused to oscillate in and at an identical phase/frequency.
The distance l may range from 1 μm to 10 mm. There is the
advantage that the frequency of the oscillations do not depend
upon the respective distances.

Although, in the foregoing, the distances between the
respectively adjacent nodes in Fig. 1 are all set to be equal
distances l, they need not always be equal distances. In such
a case, in the steady state, the oscillations of the
respective ring oscillators will have a substantially
identical frequency, but they will not have an identical
phase. The respective ring oscillators oscillate in
synchronism while keeping phases $\delta 1$ - δn (if the distances

between the respectively adjacent nodes are all equal distances 1, then $\delta 1 = \delta 2 = \ldots = \delta n$ holds).

Further, although the inverters 110 - 11m, 120 - 12m, and 1n0 - 1nm constituting the respective ring oscillators are all shown in Fig. 3 to be of the same type, they need not always be of the same type. If they are not the same, the respective ring oscillators oscillate with substantially identical frequency, but not in identical phase in the steady state as in the foregoing. The respective ring oscillators oscillate in synchronism while having the phases $\delta 1 - \delta n$. To the contrary, the phases $\delta 1 - \delta n$ can be changed by adjusting the sorts (load driving capabilities, etc.) of the inverters of the respective ring oscillators. The phases $\delta 1 - \delta n$ of the respective ring oscillators can be brought into substantially identical phase by adjusting the sorts of the inverters of the respective ring oscillators through the utilization of such a property, even when all the distances between the respectively adjacent nodes are not set at the equal distances 1.

In general, since the inverters 11m - 1nm need to drive the nodes 101 - 10n and the wiring line connecting them, each of them requires a load driving capability being comparatively high (for which the gate widths are enlarged in the case of the CMOS transistors). For lowering power dissipation, accordingly, it is effective to make the load driving capabilities higher in the order of, for example, the inverters 110, 111, ... and 11m.

Further, the numbers of stages of the inverters need not be the same in the ring oscillators. If the natural oscillation frequencies of the ring oscillators are equal to some extent, the construction of the present invention can cause the respective ring oscillators to oscillate at an identical frequency in synchronism with the phases $\delta 1 - \delta n$ kept, in the steady state.

Next, there will be explained the characteristics for the
case in which noise such as a supply voltage fluctuation or a
substrate voltage fluctuation has acted on the oscillators of
the present invention.

Fig. 3(B) illustrates circuit simulation waveforms in the
case where only the ring oscillator OSC1 has a supply voltage
different from that of the other ring oscillators. The supply
voltage of the ring oscillator OSC1 was 2.0 V, and the other
conditions were the same as those for the simulation of Fig.
3(A). It is seen that the ring oscillators OSC1 thru OSC4
oscillate in and at substantially the identical
phase/frequency in a steady state established after a while
subsequent to the point of time 0 ns.

The oscillation circuit of the present invention is
configured of a large number of ring oscillators with the
feature that, even when the supply voltages of the several
constituent ring oscillators have fluctuated, the
phase/frequency of the whole oscillation circuit hardly
changes (in the case where the ring oscillators have the
phases δ1 - δn in the steady state involving neither the supply
voltage fluctuation nor the substrate voltage fluctuation,
they function to keep the phases against the supply voltage
fluctuation and the substrate voltage fluctuation).

This effect becomes greater with an arrangement in which
the supply voltage fluctuation having acted on the ring
oscillator does not influence the supply voltages of the other
ring oscillators. In general, the supply voltage fluctuation
in an integrated circuit arises in a local place. Therefore,
in a case where a power source is shared by a plurality of
ring oscillators, the longer distance 1 is better. Further,
it is preferable that the respective ring oscillators do not
share the power source, as much as practical. By way of
example, separate supply voltage generators or supply voltage

stabilizers may well be employed for the respective ring oscillators.

Although the effect of the present invention concerning the supply voltage fluctuation has been mentioned in the foregoing, the same holds true of the substrate voltage fluctuation.

Fig. 4 illustrates an embodiment of the present invention which takes advantage of the above discussed noise immunity considerations, according to the present invention. As compared with the embodiment of Fig. 1, the embodiment in Fig. 4 differs in the point that the respective ring oscillators OSC1 - OSCn are configured of pairs of ring oscillators (OSC1a, OSC1b) - (OSCna, OSCnb). Further, the ring oscillator pairs are connected to different supply voltages VDD1a - VDDna as well as VSS1a - VSSna and VDD1b - VDDnb as well as VSS1b - VSSnb.

The probabilities at which the noise such as the supply voltage fluctuations are simultaneously involved in the supply voltages VDD1a - VDDna as well as VSS1a - VSSna and the supply voltages VDD1b - VDDnb as well as VSS1b - VSSnb, are low owing to the localities of the noise. It is therefore possible to suppress the fluctuations of oscillation frequencies and phases at nodes 401 - 40n as are attributed to the supply voltage fluctuations, the substrate voltage fluctuations, etc.

The effect of the present invention as stated above resembles the effect of a so-called bypass capacitor (decoupling capacitor) which is interposed between supply voltages in order to suppress supply voltage fluctuations. The pass capacitor functions to hold a predetermined potential in a case where noise exists in a signal having a predetermined potential (the potential termed the supply voltage) in the state in which the noise does not exist. On the other hand, the oscillator of the present invention functions to hold the predetermined oscillation

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frequency/phase in the case where noise exists in the signal having the predetermined frequency/phase in the steady state in which the noise does not exist.

Although inverters of the single-end input/output type are employed in the embodiments of Figs. 1 thru 4, differential inverters each having a differential input/output, OSC1d - OSCnd may well be employed as illustrated in Fig. 5 (the detailed circuit example of the differential inverter is depicted in Fig. 11 of the prior-art example A, and shall be omitted from illustration). In this case, the differential inverter has the oscillation outputs of a positive logic output and a negative logic output, so that equivalents to the nodes 101 - 10n in Fig. 1 become nodes (501a, 501b) - (50na, 50nb), which form dual rails.

Besides, although the ring oscillators are interconnected by using a particular one of the oscillation in the embodiments of Figs. 1 thru 5, they may well be interconnected using a plurality of oscillation nodes (having different phases) of each of the oscillators as illustrated in Fig. 6. In Fig. 6, two nodes of each ring oscillator are used for the interconnections as shown at 601a - 60na and 601b - 60nb. Since the degrees of coupling among the ring oscillators are intensified more than in the case of the connection aspect of Fig. 1, the noise immunity is enhanced.

Figs. 7 and 8 illustrate embodiments of the invention which differ from the former embodiments with respect to the connection of the oscillators. As compared with the embodiment of Fig. 1, the embodiment of Fig. 7 features the nonexistence of a wiring line part which directly connects the ring oscillators OSC1 and OSCn. On this occasion, even in the case where all of the distances between the respectively adjacent ones of the nodes 101 - 10n are the equal distances 1 and where all of the ring oscillators OSC1 - OSCn have the same characteristics, the ring oscillators OSC1 - OSCn do not

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oscillate in an identical phase though they really oscillate at an identical frequency. Herein, the ring oscillators OSC1 - OSCn oscillate in synchronism while keeping phases δ1 - δn. The phases δ1 - δn can be made identical, not only by adjusting the distances between the respectively adjacent nodes, but also by adjusting the sorts (load driving capabilities, etc.) of the ring oscillators OSC1 thru OSCn. By way of example, the load driving capability of each of the ring oscillators OSC1 and OSCn at opposite ends of the oscillation circuit may be set to half the capability of the other ring oscillators.

Fig. 8 illustrates an embodiment in which the ring oscillators are connected together by a conductive wiring in the shape of an xq mesh. The mesh connection is useful for the practical application of the invention, however various connection aspects are considered to be part of the invention, and any connection aspect may be employed as long as the ring oscillators oscillate in synchronism as a result of the connection configuration. According to the invention, a plurality of oscillators which have a natural oscillation frequency that are substantially the same, are connected through nodes of the ring oscillators so that the oscillators oscillate at a substantially identical frequency. As a result, by the arrangement of Fig. 8, an effect which is similar to that of each of the embodiments illustrated in Figs. 1 thru 4 is attained. In the ensuing description, embodiments employing the oscillator or oscillation circuit of the present invention shall be discussed using the embodiment of Fig. 1 for the sake of brevity.

Fig. 9 illustrates an embodiment of the invention in which clocks are fed to a plurality of logic circuits by the use of the oscillator of the present invention. LOG1 - LOGn denote the logic circuits, while 711 - 71n denote buffers. In comparison with the embodiment of Fig. 1, the buffers 711 -

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71n are connected to nodes 701 - 70n which correspond to the nodes 101 - 10n in Fig. 1, and the outputs 721 - 72n of these buffers are respectively fed to the logic circuits LOG1 - LOGn. As stated before, the ring oscillators oscillate at a substantially identical frequency and at a substantially identical phase at the nodes 701 - 70n (although the ring oscillators can oscillate with phases $\delta 1$ - δn as stated before, they are assumed to be connected to provide for oscillations of identical phase, for the sake of brevity). Thus, clock signals having no skew can be fed to the logic circuits LOG1 - LOGn. Further, clock signal in which little jitter occurs can be fed owing to the noise immunity as stated before. Of course, the buffers 711 - 71n may well be omitted. When the buffers 711 - 71n are existent, the propagation of noise from the logic circuits LOG1 - LOGn to the oscillator can be suppressed.

As seen from Fig. 3(B), skew at the nodes 701 - 70n in the presence of noise is less after some time period has lapsed subsequent to changes in the potentials of the nodes. Accordingly, the buffers 711 - 71n that are connected to the nodes 701 - 70n should preferably be Schmitt inputs. Thus, the skew of the outputs of the buffers 711 - 71n can be decreased.

In the embodiment of Fig. 9, the phases of the clock signals 721 - 72n input to the respective logic circuits LOG1 - LOGn can be adjusted in the direction of delaying them individually, by adjusting the delay times of the corresponding buffers 711 - 71n.

Fig. 10 illustrates an embodiment in which the phases of the clocks 721 - 72n to be fed to the respective logic circuits can be further adjusted in the direction of advancing them. Oscillation nodes (831a, 831b, 831c, ...) - (83na, 83nb, 83nc, ...) which differ from oscillation nodes 801 - 80n interconnecting the ring oscillators are selected, and the

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selected oscillation nodes are connected to the buffers 711 -
71n. By way of example, the oscillation node 831a oscillates
in a phase which is earlier than that of the oscillation node
801 for one inverter stage (the phase is earlier by 360/p
degrees under the assumption that the ring oscillator is
configured of p stages of inverters of the same sort).
Accordingly, when a clock is fed from the oscillation node
831a to the logic circuit LOG1 by the use of buffer 711, a
phase thereof is earlier than that of the clock of a logic
circuit as generated through the buffer from the oscillation
node 801.

Fig. 11 illustrates an embodiment in which the
oscillation circuit of the present invention is applied to the
voltage-controlled oscillators (VCOs) of a PLL. VCO1 - VCOn
denote the voltage-controlled oscillators, and fint1 - fintn
indicate the output signals thereof. 901 - 90n indicate
buffers, while N1 - Nn indicate clock distribution networks.
In comparison with the embodiment of Fig. 7, the voltage-
controlled oscillators VCO1 - VCOn correspond to the ring
oscillators OSC1 - OSCn, and an oscillation-frequency control
signal VC therefor is controlled by a PLL structure, thereby
to construct a phase-locked loop PLL1. In addition, global
clocks 911 - 91n being the outputs of the buffers 901 - 90n
are connected to the clock distribution networks N1 - Nn.

Although for the sake of brevity, the connection of the
voltage-controlled oscillators VCO1 - VCOn is the same as that
shown in Fig. 1, any of the connection types shown in Figs. 4
thru 8 can be employed. Further, as compared with the prior-
art example in Fig. 2, the embodiment in Fig. 11 does not show
any circuit elements corresponding to the 1/2 frequency
divider DIV2, but such elements may be connected at stages
preceding or succeeding the buffers 901 - 90n if necessary.

Circuit examples of each of the oscillators VCO1 - VCOn
are illustrated in Figs. 12(A) and 12(B). Fig. 12(A) shows an

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oscillator configured of inverters 1000 - 100m each having a single-end input/output. The delay time of each inverter changes depending upon the value of the oscillation-frequency control signal VC, whereby the oscillation frequency of the oscillation output fint1 changes depending upon the value of the oscillation-frequency control signal VC (a detailed circuit example of the inverter is depicted in Fig. 4 of the prior-art example A, and therefore its detail is omitted from illustration).

On the other hand, Fig. 12(B) shows an oscillator which is configured of differential inverters 1010 - 101m each having a differential input/output. In the same manner as in Fig. 12(A), the delay time of each differential inverter changes depending upon the value of the oscillation-frequency control signal VC, whereby the oscillation frequencies of the oscillation outputs fint1 and /fint1 change depending upon the value of the oscillation-frequency control signal VC (a detailed circuit example of the differential inverter is depicted in Fig. 11 of the prior-art example A, and therefore its detail is omitted from illustration).

Fig. 13 is a detailed diagram of the clock distribution network N1 shown in Fig. 11. 1100 - 110k indicate clock distribution lines, while 1110 - 111k indicate local buffers. The lengths of the respective clock distribution lines 1100 - 110k are set on a chip layout so that lengths from the global clock 911 to the respective local buffers 1110 - 111k may become equal. Accordingly, the characteristics of the local buffers 1110 - 111k are substantially identical (hereinbelow, termed "matched"). Furthermore, in the absence of noise, the skews of local clock outputs out1 - outk become zero.

Since the voltage-controlled oscillators VCO1 - VCOn are fed with an identical oscillation-frequency control signal VC, the oscillation outputs fint1 thru fintn thereof oscillate with a substantially identical frequency/identical phase as

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stated before (although the voltage-controlled oscillators
VCO1 - VCOn can oscillate with phases δ1 - δn as stated in
conjunction with the embodiments shown in the figures up to
Fig. 8, they are assumed to be connected to provide for
oscillations of substantially identical phase, for the sake of
brevity here). Accordingly, the local clock outputs out1 -
outk oscillate at the substantially identical frequency and
phase. Furthermore, since noise immunity similar to that
achieved in the embodiments illustrated in the figures before
Fig. 10 is attained, there is substantially no increase in the
skew/jitter of the outputs due to supply voltage fluctuations
or substrate voltage fluctuation.

Fig. 14 illustrates an embodiment in which the PLL of
Fig. 11 is applied to a microprocessor that requires high
performance from the PLL, even among the semiconductor
integrated circuit devices. Numeral 1200 designates the
microprocessor, numerals 1201 - 1203 designate logic circuit
blocks, and constituents 1211 - 1213 correspond to the clock
distribution networks in Fig. 11. The functions of the logic
circuit blocks are not especially restricted. The logic
circuit block may be either a data path with an arithmetic
unit etc. built therein, or a memory such as cache or a
controller therefor.

Global clocks 1231 - 1233 are output from the phase-
locked loop PLL1. The global clocks 1231 - 1233 are
distributed into local clocks 1241 within the respective logic
circuit blocks by the clock distribution networks 1211 - 1213.
Lastly, the local clocks 1241 are fed to the clock input units
of circuits such as latches 1220.

As in the embodiment of Fig. 11, there is substantially
no increase in the skew/jitter of the local clocks 1241 due to
supply voltage fluctuations or substrate voltage fluctuation.
Further, the voltage-controlled oscillators VCO1 - VCOn within
the phase-locked loop PLL1 are sporadically situated in the

chip and are arranged near the logic circuit blocks to which they are allotted, whereby paths from the clock outputs of the voltage-controlled oscillators VCO1 - VCOn to the circuits, such as latches to use the corresponding clock outputs, can be shortened (the path includes, e. g., the global clock 1231, clock distribution network 1211 and local clock 1241 in Fig. 14). When the path is shortened, a delay time which is involved therein can be shortened. It is therefore possible to mitigate the influence which skew or jitter having occurred in the path exerts on the performance of the whole clock distribution system.

In an arrangement (hereinbelow, called the "multiple PLL scheme") wherein a clock feed range within a chip is split in a large number and wherein independent PLLs are respectively disposed for the resulting clock feed subranges, the clock skew between the independent clock feed subranges becomes TskewG + 2*TskewL + 2*Tjitter, where TskewL denotes the skew within each clock feed subrange, Tjitter denotes the jitter of the PLL, and TskewG denotes the skew of the reference clock having occurred up to each PLL. With the arrangement of the present invention, the clock skew becomes 2*TskewLN + TjitterN where TjitterN denotes the jitter of the global clock output from the phase-locked loop PLL1, and TskewLN denotes the skew of the corresponding one of the clock distribution networks 1211 - 1213. Even when TskewL = TskewLN is assumed, by the present invention the clock skew can be decreased. In actuality, TjitterN < Tjitter holds for the PLL of the present invention as stated before, so that the arrangement of the present invention can sharply reduce the clock skew.

Furthermore, a chip area can be made smaller by the scheme of the present invention in which a larger number of VCOs than in the multiple PLL scheme are sporadically situated in the chip and are synchronized.

Although the embodiments in each of which the external clock and the internal clock are synchronized using the PLL scheme have been mentioned in the foregoing, a delayed locked loop (DLL) scheme may well be employed. By way of example, the present invention is readily applied to a DLL in such a way that the DLL is constructed by replacing the ring oscillators in Fig. 1 with delay lines.

Fig. 15 illustrates such an embodiment. Further, Fig. 16 illustrates an embodiment in which a DLL is constructed by laying the delay lines in Fig. 15 as variable delay lines. As compared with the embodiment of Fig. 11, the embodiment of Fig. 16 differs in the point that the reference clock fext is input to the variable delay lines VDL1 - VDLn. Otherwise, it is obvious that the embodiment of Fig. 15 is applicable to each of the embodiments of the present invention illustrated in Figs. 2 thru 14.

Each of the foregoing embodiments corresponds to the case where the present invention is applied within a single chip, but obviously it can be expanded to embodiments of semiconductor integrated circuit devices each of which includes a plurality of chips. By way of example, the present invention is readily applied to a case where, as in Fig. 14, the logic circuit blocks and the voltage-controlled oscillators VCOs allotted thereto are constructed using respectively separate chips, or a case where, as in Fig. 1, the ring oscillators are constructed using respectively separate chips.

In addition, none of the foregoing embodiments includes a method for lowering power dissipation, such as so-called gated clock. The present invention, however, is readily applied to a case, for example, where the buffers 711 - 71n in Fig. 10 are altered into and constructed as gate circuits. Although there are various different methods, the present invention is not especially restricted to such methods, and one such method

for lowering power dissipation is provided by an arrangement shown in Fig. 17(A).

In Fig. 17(A), an arrangement is shown using switches in which only part of the many oscillators used in the present invention need be operated at any one time in order to selectively lower power dissipation. Fig. 17(B) shows a preferred embodiment of one of the switches shown in Fig. 17(A).

As shown in Fig. 17(A), the switches are connected to the wiring lines interconnecting the ring oscillators in the embodiment where the ring oscillators are connected in a mesh of n×q, according to the embodiment of Fig. 8. The switches may be, for example, CMOS switches as shown in Fig. 17(B), although not limited thereto.

When all of the ring oscillators are to be operated, all of the switches are turned on. Meanwhile when, for example, it is desired that only the ring oscillators OSC11, OSC12, OSC21, OSC22 are operated and the other oscillators are not operated, switches SW1213, SW2223, SW2232, SW2131 are turned off. By turning off the switches SW1213, SW2223, DE2232, SW2131, the not-operating ring oscillators do not influence the ring oscillators OSC11, OSC12, OSC21, OSC22. In order to reduce the power consumption by supplying clock signals to only part of the circuits, for example, the structure and control method of the invention can be used.

In the foregoing examples, although it is premised that the frequency of the ring oscillators is controlled by the oscillation-frequency control signal, the ring oscillators may be the ones whose frequency is determined by a clock inputted from outside. This can be realized by, e.g. adopting a PLL structure. Fig. 18 shows a structure wherein instead of the to the oscillators OSC11-OSCqn used in the embodiment of Fig. 8, there are provided phase lock loop circuits PLL11 to PLLqn that receive a clock from outside (not shown).

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The PLL circuits shown in Fig. 18 have an input and an output respectively connected to separate first and second conductive wirings, each in the shape of a mesh. The phase and frequency of the outputs is synchronized for each of the outputs of the PLL circuits that is connected to the first conductive wiring. On the other hand, a reference clock signal is input to each of the PLL circuits connected to the second conductive wiring. The second conductive wiring of Fig. 18 is used to distribute the reference clock signal as an input to each of the PLLs with the same frequency and phase, so the shape of the wiring is not limited to the mesh shape shown in the figure, but may take another form so long as this function is performed. If there is a slight variation in the frequency of the reference clock signal input through the first conductive wiring to each of the PLL circuits, there is substantially no variation in the output clock signal from each of the PLL circuits because of the effect achieved by the present invention wherein each of the oscillators of the PLL circuits are connected together by the second wiring.

As compared with the previous embodiments (Figs. 8 and 11, for example) in which the frequency control signal for the oscillators is distributed over the entire chip, the present embodiment uses the reference clock signal as an output to the PLL circuits so that distribution of a frequency control signal is not required. Accordingly, the present embodiment enables the distribution of the input reference clock signal according to the known technology of distributing a clock signal. Further, according to this embodiment, a stable output clock signal is distributed that does not vary between each PLL circuit even when there are variations in the phase of the reference clock signal input to each of the PLL circuits. Accordingly, the clock signal provided that is distributed according to this embodiment is not subject to variations due to noise.

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Fig. 19 illustrates an example of each of the PLLs, PLL11 to PLLqn, used in Fig. 18. The symbols used in Fig. 19 are identical with those of Fig. 2, and therefore further description thereof will be omitted.

Although some of the foregoing embodiments employ ring oscillation circuits in which a plurality of inverters are connected in a ring shape in multistage fashion, the present invention is not restricted to such a construction. Alternatives to the ring oscillation circuit may be employed in the present invention. It suffices that the oscillation frequency and phase of the oscillation circuit can be adjusted using the oscillation output thereof as input/output lines, and that a plurality of such oscillation circuits connected as described can oscillate in synchronism.

Further, in each of the foregoing embodiments, the semiconductor process, the transistor structure, etc. used in the present invention is not particularly described. A CMOS process may be employed, and an SOI transistor made from an SOI wafer may be employed. No specific limitations are placed on the type of the supply voltages or the sorts thereof.

As set forth herein, according to the present invention, it is possible to provide clock signals and a clock distribution circuit or system of circuits having low skew and low jitter to logic circuits and memory circuits of a microprocessor or the like. Further, a semiconductor integrated circuit device of high speed can be provided as a result of the stable clock signal that is able to be generated and distributed in accordance with the present invention.

While preferred embodiments have been set forth with specific details, further embodiments, modifications and variations are contemplated according to the broader aspects of the present invention, all as determined by the spirit and scope of the following claims.